RESEARCH ON SiC FOR IMPROVED RELIABILITY

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ABSTRACT. Significantly improved high-temperature reliability of SiC metal-insulator semiconductor (MIS)devices has been achieved with both thermally grown oxides and by using a stacked dielectric consisting of silicon oxide-nitride-oxide (ONO).Capacitors of p-type 6H-SiC,n-type 6H-SiC and n-type 4H-SiC were fabricated with a variety of insulators. The best performance was accomplished only with insulators incorporating silicon dioxide. A new thermal oxidation process of growing a dry oxide then following with a wet re-oxidation anneal produces an oxide with the dielectric strength of a dry oxide and the high-quality interface of a wet oxide. MIS field effect transistors (MISFET's) with a ONO gate insulator had surface channel mobilities similar to MISFET's with thermal gate oxides, and demonstrated a lifetime of 10 days at 335^{o} C and 15V bias. The lifetime of the ONO MISFET was a factor of 100 higher then for devices fabricated with deposited oxides, which had been the prior state of the art for high-temperature MISFET 's on SiC.

1. INTRODUCTION

Because of its electrical and physical properties (3,0 eV bandgap ,4 MV/cm electric field breakdown ,3,7 W/cm-k thermal conductivity ,2,0 x 10^{7}cm/s electron drift velocity),silicon carbide is a very attractive semiconductor for high-temperature ,high power and high-frequency devices [1].The ability to grow thermal oxides on SiC also gives it significant advantage over other compound semiconductors. However, the performances of metal-oxide-semiconductor (MOS) devices in SiC has been limited by poor interface quality between the oxide and SiC. With the exception of substrate crystal quality, oxide quality and reliability is the largest barrier to the commercialization of advanced SiC MIS power devices and integrated circuits [2],[3].

One approach to improving the performance of power MISFET 's is to utilize a dielectric material with a higher dielectric material with a higher dielectric constant (e) then SiO_2 Gauss ' law $(\nabla \cdot \varepsilon\varepsilon_o \vec{E} = 0)$ requires the product of the relative dielectric constant and the normal field of two materials (eE) to be constant at their interface. Therefore, a material with a dielectric constant higher than that of SiC will have a lower electric field then the adjacent SiC. Thus, a critical measure of a material 's applicability as a gate dielectric or as a gate dielectric or passivant for power devices is the product of its product of its relative dielectric constant (e)and its safe operating field (E_o).Ideally this eE_o product would exceed that for SiC. Several relevant dielectric materials that have desirable characteristics are listed in Table 1.

The first four insulators listed in Table 1 under SiC are common dielectric materials used for semiconductor applications, and their characteristics are well known. The operating field is typically limited to 20% of the critical field by

electrons tunneling from the substrate into the material. On SiC, A1N exhibits a large "avalanche" current around 10-12 MV/cm that is not destructive to the material. For this reason, the operating field of A1N on SiC is expected to be higher fraction of the critical field.

A1O:N is generated by thermal oxidation of A1N,and is not significantly different than Al_2O_3 [4].The critical and operating fields are approximated for this material.

Table 1

Material	Dielectric Constant	Critical Field (MV/cm)	Operating Field (MV/cm)	εE_0 (MV/cm)
SiC	10	3	3	30
Thermal SiO_2	3.9	11	2	7.8
Deposited SiO_2	3.9	11	2	7.8
Si_3N_4	7.5	11	2	15
ONO	6	11	~2	~12
AlN	8.4	10-12	~3‡	~30
AlO:N	12.4[4]	8‡	~1‡	~12
$Si_xN_yO_z$	4-7	11	~2	~8-14
(Ba,Sr)TiO_3	75-250*	2‡	~0.1[7]	~8
TiO_2	30-40	6	~0.2‡	~4
Ta_2O_5	25	10[6]	~0.3[6]	~7.5

(Ba,Sr) TiO_3,TiO_2,and Ta_2O_5 have been of considerable interest recently for silicon DRAM applications because of their extremely high dielectric constants, and theoretically could improve SiC device performance [5].However ,these materials have leakage currents and a temperature/time resistance degradation at very low fields which lowers their operating fields considerably [6]-[9]. Although high dielectric constants may make these materials seem quite promising, the leakage currents and constraint on the operating field are significant detractors.

Part of the challenge associated with investigating alternative dielectrics for use as a high-temperature, high-voltage passivant or gate dielectric is the wide assortment of materials from which to choose. The materials in Table 1 with figures of merit exceeding that of silicon dioxide (εE_0 > 8MV/cm) were investigated. MIS capacitors were used as a preliminary instrument to determine which materials had the most promise for use as a MISFET gate dielectric. Four insulators were chosen to be fabricated into a set of 6H-SiC planar MISFET's.

2. FABRICATION

MIS capacitors were fabricated on SiC epitaxial layers grown on SiC substrates. N-type 4H-SiC,n-type 6H-SiC and p-type 6H-SiC substrates had epitaxial layers grown with a doping level of 5-8*10^{15} cm^{-3} .Seven dielectrics were investigated :two different thermally grown silicon dioxide layers, low pressure

chemical vapor deposition (LPCVD) silicon dioxide, silicon nitride, oxide-nitride-oxide (ONO) layers,A1N,and A1O:N.Where possible, the insulator thickness was determined by ellipsometry ; the others (ONO,A1O:N,A1N) were etched and measured via profilometry.

The following methods were used to create the insulating layers of the MIS capacitors.

- State-of-the-art thermal SiO_2 (identified as "SOA SiO_2") was grown in a standard oxidation furnace. The oxidation ambient depended on the wafer type : P-type at 1025^0C in a wet ambient [10], followed by a 950^0C "re-oxidation" anneal [11];N-type at 1200^0C in a dry ambient followed by an argon anneal at the same temperature. The average oxide thickness was 66 nm for the p-type oxidation and 48.6 nm for the n-type.
- Dry-wet SiO_2 (a second set of thermal oxides) were grown at 1100^0C in a dry ambient, followed by a 950^0C wet re-oxidation anneal with the ramp down in a wet ambient. This process was created with the hopes of having the higher dielectric breakdown strength of a dry thermal oxide [12] and the better interface of a wet thermal oxide [10],[11] for p-type samples. The average oxide thickness was 52.1 nm.
- LPCVD SiO_2 was deposited using a standard low temperature oxide recipe, which was then processed with a 950^0C wet re-oxidation anneal [10],[11].The average oxide thickness was 53.4 nm.
- ONO layers were created with a three-step process. First, high-quality thermally grown silicon dioxide was grown in the oxidation furnace to a thickness of 10nm.Then a 60-nm silicon nitride layer was deposited via LPCVD. This layer was then oxidized in a wet ambient at 950^0C for 3 h to form the top 5-10 nm oxide. Total thickness of the stacked dielectric was about 70nm.Altough this thickness results in accumulation capacitance values similar to the thinner oxides, due to the higher dielectric constant, the actual physical thickness (as determined via profilometry) is used in all field calculations.
- A1N was metal-organic chemical vapor deposition (MOCVD) deposited. The aluminum nitride thickness was about 53.5 nm.
- A1O:N was created by first depositing 50nm of A1N via MOCVD, then oxidizing the material at 1100^0C in a dry oxygen ambient for 1 h [4].The A1O:N was about 86.5 nm thick.

After the insulator was deposited or grown, a 200-nm molybdenum layer was sputter deposited on the front of the wafer and topped with a 50-nm layer of gold. Molybdenum is stable at high temperatures on SiO_2,and the gold capping layer eliminates Mo oxidation. The metal was patterned with photoresist and etched with a two-step wet etch. The gold was etched first with a potassium iodide commercial gold etchant, then the molybdenum was etched in a phosphoric/acetic acid commercial aluminum etchant at 35^0C.Finally,any insulator on the back of the wafer was removed via reactive ion etch. The capacitors were 200- or 400-µm squares (as patterned), and had actual areas of 0.0039 and 0.00157 cm^2, respectively.The larger capacitors were used for

interface characterization, and the smaller capacitors for breakdown measurements.

3. INTERFACE QUALITY

For high-temperature, high-field device passivation applications, a dielectric must have high reliability. However, this is not enough to dictate its applicability for a gate layer of an MIS device. For this application, it is critical that charged bulk defects and electrically active interface defects must be minimized.

High-frequency capacitance-voltage (C-V) measurements were used to determine the room temperature flatband voltage, which is used to calculate the net oxide charge density. Any difference between the actual voltage at which flatband capacitance occurs and the ideal value, accounting for metal-semiconductor work functions, determines the net oxide charge. For wide bandgap semiconductors, such as SiC, the calculated charge density includes contributions from mobile ions, interface states and border traps, many of which appear fixed at room temperature.

The MIS capacitors were characterized using a Hewlett Packard 4284A LCR meter. An initial 500 kHz high-frequency CGV sweep is taken at room temperature in a darkbox unilluminated throughout the measurements. The capacitors were biased from depletion (0 V) into accumulation (-7 V for p-type or +7 V for n-type samples) and immediately back to depletion (0 V). If the initial sweep is did not go into accumulation, the voltage range was increased appropriately and a fresh device measured. The voltage sweep is done with 0.25 V steps, and is swept at approximately 0.5 V/s. The flatband capacitance and voltage are determined from the accumulation to depletion sweep. The difference between the flatband voltage and the metal-semiconductor work function difference (typically -2.35 V for 6HP, 0.15 V for 6HN and 0.30 V for 4HN SiC doped ~$5*10^{15}$ cm^{-3}) subsequently determines the net oxide charge.

The accumulation capacitance was typically around 100 pF, but obviously varied with the dielectric constant and thickness of the material. Backside contact was made to the bare SiC via a gold-plated vacuum wafer-chuck .A large (~$1cm^2$) frontside capacitor was used to make a contact to the substrate in parallel with contact to the back of the wafer, which was found to minimize any effects from epitaxial layer nonuniformities or series resistance.

The C-V curves for the 6H p-type and 4H n-type samples are shown in fig.1.

1.) The n-type Si_3N_4 capacitors have an accumulation capacitance of about 170 pF while the p-type have less than 40 pF, seen at -3.5 V. The p-type samples have significant AC conductance, which prevents the capacitance from being properly measured. The original measurement of the Si_3N_4 p-type samples was swept to -7 V ,but the conductance was so high the measurement became meaningless above -3.5 V. The sweep was repeated to -3.5 V and back on a

fresh device. No net oxide charge could be determined from this sample. The AC conductance may be related to dc leakage ,but was lower than could be detected via dc measurements (500pA).

2.) Large hysteresis is seen on many samples, and is more pronounced on the n-type samples. This hysteresis is undesirable, and we believe it results from interface states. Similar hysteresis is seen on Si MOS capacitors that have been annealed in forming gas.

3.) Varying slopes. The slope of the C-V curves will be affected by the doping of the SiC epitaxial layer and the interface state density. The doping of the SiC layers was 5-8*10^{15} cm^{-3}, which would produce no more than a 20% difference in the ?C/? V slopes. The differences in the C-V slope result from the various interface state densities.

4.) Differing accumulation capacitances. There are several samples where the accumulation capacitance appears to be different on the p-type than for the n-type samples. This is partially due to differences in the thickness of the insulator (5-10% variation).Differences larger than this result from the C-V stretch-out created by the interface state densities, which makes it difficult to reach true accumulation, as evidenced by the C-V curves not fully flattening in accumulation. The exception is the SOA oxides separately, resulting in a 66-nm oxide on the 6H p-type and a 49-nm oxide on the 4H n-type sample.

5.) Large flat-band voltage variations. The large flat-band variations can be quantified into an effective, or net oxide charge. It is important to remember that for wide bandgap semiconductors, such as SiC, the calculated net oxide charge density includes contributions from mobile ions, interface states and border traps. Although several insulators are deposited, and one might expect the bulk oxide charge to be identical between the different substrates, the net oxide charge is dominated by interface states, which are affected by the semiconductor/insulator interface and will vary with crystal structure and dopant type. Much of the large flat-band variation is due to differences of more than two orders of magnitude in interface state densities.

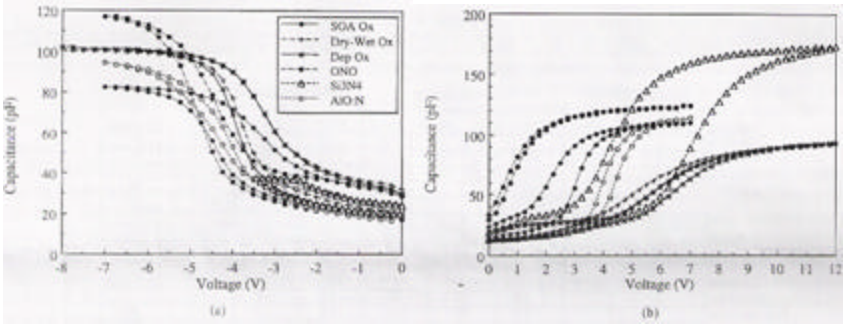

Fig.1. Capacitance versus voltage curves. (a) 6H p-type capacitors. The voltage was swept from 0 V negatively and back.(b) 4H n-type capacitors. The voltage was swept from 0 V positively and back. The hysteresis is always negative for negative bias (p-type) and positive for positive bias (n-type).

The conductance technique [13]-[15] was used at 250^0C to measure the interface state density. The high temperature of the measurement was necessary to activate the interface states that reside deep in the 3 eV wide SiC bandgap. Conductance-capacitance-frequency sweeps were taken with a Hewlett Packard 4284A LCR meter at 250^0C,and the G_p/? *-f* data was fit to theoretical curves.Fig.2. demonstrates the conductance technique measured on a p-type

6H-SiC MOS capacitor thermally oxidized at 1100^0C in a dry ambient followed by a 950^0C wet re-oxidation anneal.(This oxidation has been repeated on six different wafers, all of which had minimum interface state densities between 2 and $5*10^{10}$ cm^{-2} eV^{-1}.)

The traditional peaks obtained with this measurements technique are exhibited in Fig.2(a).The interface state distribution across the bandgap is shown in Fig.2(b).Although the conductance technique measures the interface state density distribution over a portion of the bandgap, the minimum value is used for comparison. The minimum always occurs nearest mid-gap, which corresponds to the lowest frequency peak. The accuracy of comparing the minimum interface density is limited by interface state densities plummeting toward mid-gap, and the difficulty in controlling the precise position in the bandgap.

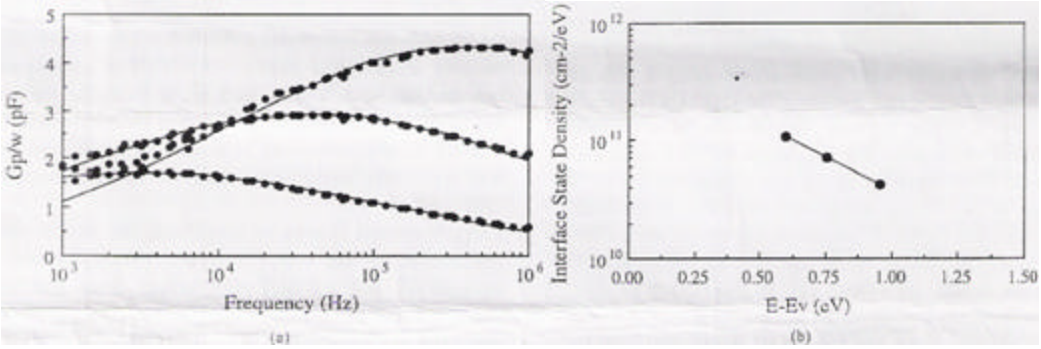

Fig.2. Conductance technique data taken at 250^0C for a 1100^0C dry oxide followed by a 950^0C wet re-oxidation anneal o0n p-type 6H-SiC.(a) The characteristic peaks are demonstrated. The measured points are represented by circles, and the theoretical fit is the solid line. The voltages applied to the capacitor were -2.4, -2.2, and -2.0 V. The bandbending variation was 3.2 kT/q. (b) Interface state distribution in the bandgap. The measurement closest to mid-gap corresponds to an interface state density of $4.2*10^{10}$ cm^{-2}/eV and a time constant (T_p)of $1.3*10^{-4}$ s.

On p-type samples, the net oxide charge and interface state densities are the lowest on thermal oxides and the LPCVD oxides. For the n-type samples, the net oxide charge are significantly lower on the ONO and A1O:N samples ,while the interface states were lowest on the ONO capacitors. The A1N and A1O:N insulate at room temperature, but at 250^0C, which is necessary to measure interface states, the samples leaked too much for a measurement to be obtained.

From the accumulation capacitance and the insulator thickness, the empirical relative dielectric constants of the various materials can be estimated. With the exception of the A1O:N,the relative dielectric constant determined from the accumulation capacitance agreed fairly well with the expected values. This agreement confirms the insulator thickness.

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